CORRECTED VERSION

(19) World Intellectual Property **Organization**

International Bureau





(43) International Publication Date 24 June 2004 (24.06.2004)

PCT

(10) International Publication Number WO 2004/053824 A1

(51) International Patent Classification⁷: 3/32, 3/36

G09G 3/20,

(21) International Application Number:

PCT/IB2003/005321

(22) International Filing Date:

21 November 2003 (21.11.2003)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data: 0228479.2

6 December 2002 (06.12.2002) GB

(71) Applicant (for all designated States except US): KONIN-KLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

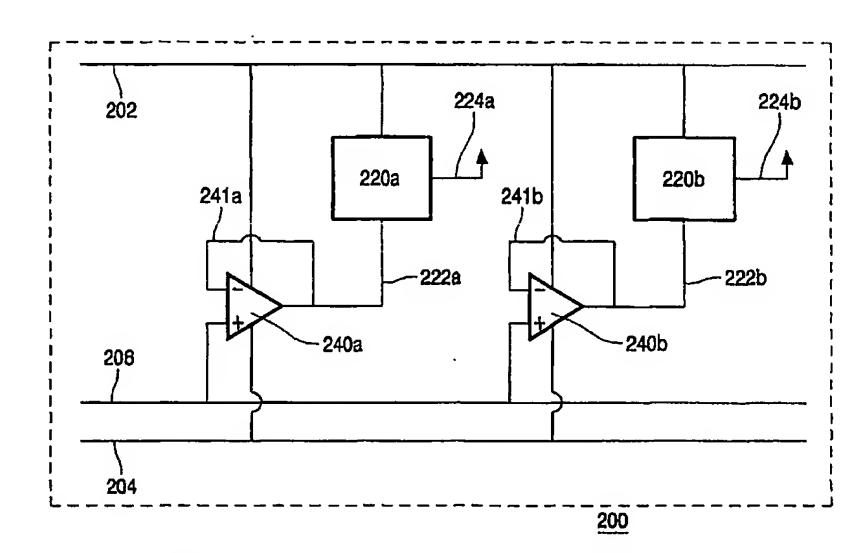
(75) Inventors/Applicants (for US only): KNAPP, Alan, G. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

DEANE, Steven, C. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

- (74) Agent: WHITE, Andrew., G.; Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT ARRANGEMENT, INTEGRATED CIRCUIT, MATRIX ARRAY OF CIRCUITS AND **ELECTRONIC DEVICE**



(57) Abstract: An IC arrangement (200) has a plurality of IC modules (220a, 220b), the individual IC modules (220a, 220b) being coupled between a first power line (202) and a second power line (204) via a voltage generator (240a, 240b). The voltage generators (240a, 240b) are powered via the first power line (202) and the second power line (204) and are arranged to regenerate a reference voltage on a reference power line (106) for providing the IC modules (220a, 220b) with the regenerated voltage on respective internal power lines (222a, 222b). A feedback loop (242a, 242b) from the internal power lines (222a, 222b) to the voltage generator (240a, 240b) ensures that the voltage on the internal power lines (222a, 222b) remains substantially constant, even if substantial current fluctuations on the first power line (202), the second power line (204) or the internal power line (222a, 222b) occur. The IC arrangement (200) is particularly suitable as a driver circuit for a matrix array device.



053824